IN THE CLAIMS:

1. (Currently amended) A pulse width limiting circuit, comprising:

a clock signal correction block configured to receive a conditioned clock signal and generate a corrected clock output signal, wherein the clock signal comprises a train of clock pulses, each of which has a rising clock edge, a falling clock edge and a variable width;

a block delay module, coupled to the clock signal correction block, configured to accept an unconditioned clock signal and introduce a specified pulse width delay to thereby generate the conditioned clock signal, wherein the block delay module comprises a plurality of delay sub-blocks of fixed delay; and

a high low clock pulse shuttle circuit, coupled to the clock signal correction block, configured to accept the conditioned clock signal, wherein the high low clock pulse shuttle comprises a first field effect transistor (FET) coupled to the correction block and a second FET coupled to a conditioned clock signal output interconnect, and wherein ~~individual delay sub-blocks of the plurality of delay sub-blocks of the block delay module are disconnected and reset based on the unconditioned clock signal~~ the high low clock pulse shuttle circuit shunts the unconditioned clock signal to the block delay module if a clock pulse width of the unconditioned clock signal is outside a pulse width limit, and wherein the unconditioned clock signal is passed as the corrected clock output signal if the clock pulse width of the unconditioned clock signal is equal to or less than the pulse width limit by bypassing the high low clock pulse shuttle circuit.

2. (Previously presented) The system of claim 1, wherein the unconditioned clock signal is input to the source of a P-type FET in the high low clock pulse shuttle.

3. (Previously presented) The system of claim 1, wherein the clock signal correction block further comprises a correction unit and a leak detector unit, wherein the clock signal correction block is employed to transmit the conditioned clock signal to the high low clock pulse shuttle.

4. (Previously presented) The system of claim 2, wherein the high low clock pulse shuttle is coupled to an interconnect, wherein the interconnect is employed to convey the unconditioned clock signal.

5-6. (Canceled)

7. (Previously presented) The system of claim 1, further comprising a node to transmit the conditioned clock pulse between the clock signal correction block, the high low clock pulse shuttle circuit and a clock pulse inverter.

8. (Original) The system of claim 3, further comprising a leak detector calculating a voltage potential between two digital devices.

9. (Previously presented) The system of claim 7, wherein an uncorrected clock pulse bypasses the clock signal correction block and the high low clock pulse shuttle circuit for delivery through the clock pulse inverter.

10. (Currently amended) A method for performing a plurality of clock pulse widths limiting in clock pulses, comprising:

initiating a clock [[in]] pulse as a result of a clock cycle;

~~routing a clock pulse;~~

~~initiating a correction block;~~

~~determining a voltage leak;~~

forwarding [[a]] the clock pulse through a clock shuttle node;

injecting [[a]] the clock pulse through a block delay module in response to the clock shuttle node identifying a clock pulse width of the clock pulse as being outside a predetermined pulse width limit;

sequentially advancing a clock pulse through delay sub-blocks;

~~disconnecting and resetting individual delay sub-blocks;~~

altering a clock pulse that is greater than a predetermined pulse width; and

substantially passing through [[a]] the clock pulse by bypassing the clock shuttle node in response to the clock pulse width of the clock pulse being less than or equal to [[a]] the predetermined pulse width limit.

11. (Previously presented) The method of claim 10, wherein a clock pulse width is selected for correction by a specific state within a correction block.

12. (Original) The method of claim 11, wherein a clock pulse width is deselected for correction by a specific state within a correction block.

13. (Original) The method of claim 11, wherein a selected clock pulse is passed through a clock pulse correction block and checked by a leak detector.

14. (Original) The method of claim 11, wherein a deselected clock pulse is passed through a clock shuttle and output through a clock pulse inverter.

15. (Original) The method of claim 11, wherein a selected clock pulse is passed through a clock pulse correction block, checked by a leak detector, and input to a block delay module.

16. (Original) The method of claim 11, wherein the block delay module is conditioning the clock pulse using a series of delay sub-blocks.

17. (Original) The method of claim 11, wherein the delay sub-blocks are sequentially disconnecting and resetting as the clock pulse is passing.

18. (Canceled)

19. (Original) The method of claim 11, wherein a completely conditioned clock pulse outputs to a conditioned clock pulse dependent device.

20-21. (Canceled)

22. (Currently amended) A method of providing a pulse width limiting circuit, comprising:

providing a clock signal correction block configured to receive a conditioned clock signal and generate a corrected clock output signal; [[and]]

providing a block delay module, coupled to the clock signal correction block, configured to accept an unconditioned clock signal and introduce a specified pulse width delay to thereby generate the conditioned clock signal, wherein the block delay module comprises a plurality of delay sub-blocks of fixed delay, and wherein individual delay sub-blocks of the plurality of delay sub-blocks of the block delay module are disconnected and reset based on the unconditioned clock signal; and

providing a high low clock pulse shuttle circuit, coupled to the clock signal correction block, configured to accept the conditioned clock signal, wherein the high low clock pulse shuttle comprises a first field effect transistor (FET) coupled to the correction block and a second FET coupled to a conditioned clock signal output interconnect, and wherein the high low clock pulse shuttle circuit shunts the unconditioned clock signal to the block delay module if a clock pulse width of the unconditioned clock signal is outside a pulse width limit, and wherein the unconditioned clock signal is passed as the corrected clock output signal if the clock pulse width of the unconditioned clock signal is equal to or less than the pulse width limit by bypassing the high low clock pulse shuttle circuit.

23. (Currently amended) A pulse width limiting circuit, comprising:

a correction block circuit; [[and]]

a block delay module coupled to the correction block circuit; and

a high low clock pulse shuttle circuit, coupled to the correction block, wherein the block delay module comprises a plurality of delay sub-blocks, and wherein:

individual delay sub-blocks are disconnected and reset based on an input clock,

a clock pulse is sequentially advanced through the plurality of delay sub-blocks such that the clock pulse is altered by the delay sub-blocks if the clock pulse has a pulse width greater than a predetermined pulse width, and

the clock pulse is substantially passed through the pulse width limiting circuit if the pulse width of the clock pulse is less than or equal to the predetermined pulse width, and wherein the high low clock pulse shuttle circuit shunts the clock pulse to the block delay module if a clock pulse width of the clock pulse is outside a pulse width limit and wherein the high low clock pulse shuttle circuit is bypassed if the clock pulse width of the clock pulse is equal to or less than the pulse width limit.

24. (New) The pulse width limiting circuit of claim 1, wherein when the unconditioned clock signal has a high state, the high low clock pulse shuttle circuit is bypassed, an input to the delay sub-blocks of the block delay module has a low state and the delay sub-blocks are in a reset mode of operation with their outputs being in a low state, and wherein the conditioned clock signal input to the clock signal correction block has a high state.

25. (New) The pulse width limiting circuit of claim 1, wherein when the unconditioned clock signal has a low state, the high low clock pulse shuttle circuit outputs an input signal to the delay sub-blocks of the block delay module having a high state such that the delay sub-blocks are in a pulse width limit mode of operation, and wherein after a delay period introduced by the delay sub-blocks, an input to the clock signal correction block and an associated leak detector is placed in a low state causing the leak detector to connect the clock signal correction block to a voltage source and pull the clock output low.

26. (New) The pulse width limiting circuit of claim 1, further comprising a node coupled to the clock signal correction block, a leak detector, and the high low clock pulse shuttle circuit, wherein the node is connected to ground when the unconditioned clock signal is low such that the node is in a floating state in which it retains its last value

assuming no voltage leakage, and wherein when the unconditioned clock signal is high, any connection between the node and a voltage source is disconnected and thus, the node is pulled low.